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		APPLICABLE DIVISION
	SPECIFICATION	■ DUTY PANEL DEVELOPMENT CENTER ❑ ITFT DEVELOPMENT CENTER ☐ LCD PRODUCTS DEVELOPMENT CENTER ❑ EL PRODUCT 10N DEPT.

SPEC I F I CAT 10N FOR

Passive Matrix LCD Module

Model No.

LM161556

❑ CUSTOMER' S APPROVAL

DATE

BY

PRESENTED

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RECORDS OF REVISION

SPEC No.	MODEL No.
LC 95502	LM161556

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I DENT. DATA No.

DATA	SPEC REVISED No.	REVISED No.	REF. PAGE	SUMMARY	CHECK & APPROVAL

1. Overview

The LM161556, dot-matrix LCD module consists of a combination of a 5 X 7-dot 16-character l-line dot-matrix LCD panel, LCD driver and controller LSI mounted on a single P.C.B.
Incorporating mask ROM-based character generator and display data RAM in the controller LSI, the module is capable of efficiently displaying the desired characters under microcomputer control.

(Features)

(1) Power dissipation is extremely low because of the dot-matrix LCD panel and CMOS LSI.
(2) With the LCD panel and driver mounted on a single P.C.B., the module is very thin for ease of tacking into appliances.
(3) Allowing for being connected at general-purpose CMOS signal level , the module can be easily interfaced to a microcomputer with common 4-bit and 8-bit parallel inputs and outputs.
(4) Internal character generator RCM and RAM and display data RAM:
Character generator RCM-
5 X 7 dots, 160 kinds of characters
(alphanumeric and symbols)
Character generator ~Y-
5 X 7 dots, 8 characters
(write capability by program)
Display data RAM-
80 X 8 bits
(5) Extensive instruction set:
Display clear, cursor home, display ON/OFF, cursor ON/OFF, character blink, cursor shift, and display shift.
(6) Internal automatic reset circuit at power-on.
Refer to the separated users manual for the operating conditions .
(7) Since the module oparates from a single 5v power supply, it provides highly stable display over a wide range of temperature.

* As to the packing, refer to the separate "COMMON PACKING SPECIFICATION FOR LM16155 series".

2. Construction and Outline

Construction : 5 X 7 dots + cursor, 16-character l-line dot-matrix display module

Outline : See Fig.7.

Interface signals See Table 5.

Character pattern details : See Fig.7.

Character codes : See Table 8.

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function. Rejection criteria shall be noted in Inspection Standard (S-A-082) .

3. Mechanical Specifications

Table 1

Parameter	Specification	Unit
Outline dimensions	80(W) x 36(H) x 11 MAX(D)	mm
Effective display area	64.5(w) X 13.8(H)	mm
Display format	16 characters X 1 line	-
Character format	5 X 7 dots with cursor	-
Character size	3.07(w) X 5.73 (H)(5 X 7 dots)	mm
Dot size	0.55(W) X 0.75(H)	mm
Dot spacing	10.08	mm
Character color *	Dark blue	-
Backlight color	White	-
Weight'	Approx. 25	9 "

* Due to characteristics of the LC Material, the color vary with environmental temperature.

4. Electrical Specifications

4.1 Absolute maximum ratings

Table 2

Parameter	Symbo 1	Min.	Max.	Unit	Remark
Supply voltage(Logic)	VDD-VSS	-0.3	7	v	
Supply voltage(LCD drive)	VDD-V0	0	13.5	v	
Input voltage	VIN	-0.3	VDD+0 .3	v	
Storage temperature	Tstg	-25	70	"C	
Operating temperature	Topr	0	50	"C	

4.2 Electrical characteristics

Table 3 (Ta=25℃)

Parameter		Symbo 1	Min.	Typ.	Max.	Unit	Condition
Supply voltage(Logic)		VDD-VSS	4.75	5	5.25	V	
Supply voltage (LCD drive)		V0 -Vss		1		V	VDD=5V
Input voltage	"L"	VIL	-0.3	-	0.6	v	
	"H"	VIH	2.2	-	VDD	v	
output volt age	"L"	VOL	-	-	0.4	V	ICL=1.2mA
	"H"	VOH	2.4	-		V	-IOH=0.205mA
Input leakage current		IIL	-	-	1	uA	
Internal oscillating frequency		fosc		250		KHz	
Supply current (Logic circuit)		IDD		1.5	2	mA	VDD=5v Vo =0V
Power dissipation		Pd		7.5	10	mW	

4.3 Timing characteristics

Table 4

VDD=5.0V±5%
Ta=0~50℃

Parameter	Symbo 1	Min.	Typ.	Max.	Unit
Enable cycle time	tcycE	1000		-	ns
Enable pulse width	PWEH	450			ns
Enable rise/fall time	tEr, tEf			25	ns
RS,R/W setup time	tAS	140			ns
Address hold time	tAH	10			ns
Data setup time	tDSW	195			ns
Data delay time	tDDR			320	ns
Data hold time(write)	tH	10			ns
Data hold time(read)	tDHR	20			ns

Timing chart: See Fig.1.

4.4 Interface signals

Table 5

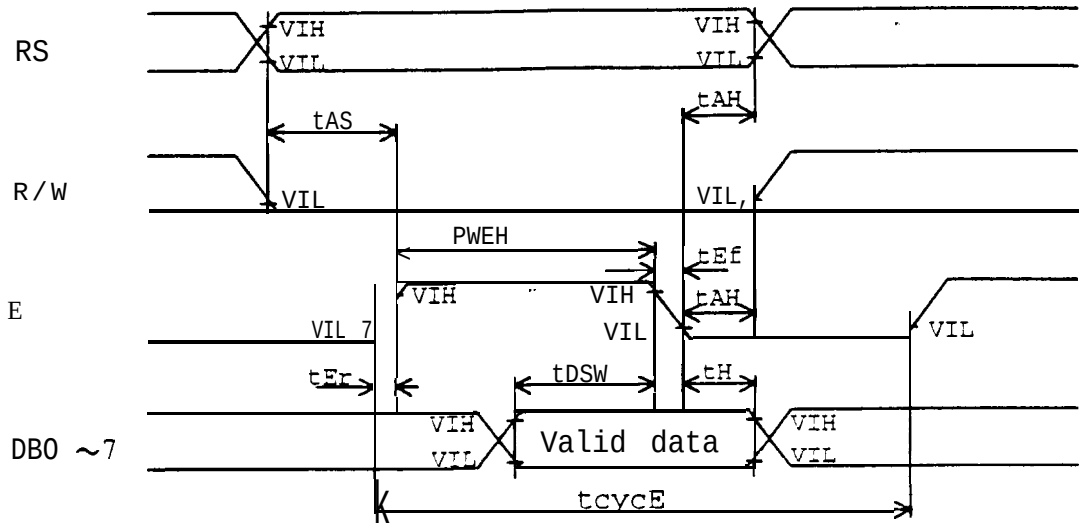
Pin No.	Symbo 1	Description	Connection
1	**Vss**	Ground potential	GND : 0V
2	VDD	Power supply	+ 5V
3	Vo	Contrast adjustment voltage	Adjust the contrast by changing the Supply voltage from 0V to 5V.
4	RS	Register select signal	Control signal inputs (For details, see section 6 and7.)
5	R/W	Read/write select signal	
6	E	Operation(data read/write enable signal)	
7	DB0	Code 1/0 data LSB	Data bus line :DB7 may also be used to check the busy flag. :Lines DB0~DB3 are not used when interfacing with a 4-bit microprocessor. (For details, see section 6 and 7.)
8	DB1	Code I/O data 2nd bit	
9	DB2	Code 1/0 **data** 3rd bit	
10	DB3	Code I/O data 4th bit	
11	DB4	Code 1/0 data 5th bit	
12	DB5	Code I/O data 6th bit	
13	DB6	Code 1/0 data 7th bit	
14	DB7	Code I/O data MSB	

4.5 Recommendable connector

Usable connector	Correspondable connector	Manufacturer
W-P5014	W-F1914	Showa Musenkogyo K.K.
5267-14A,	5264-14	Mo 1 ex
FCN-724P014-AU/S	FCN-723J014/1	Fuj itsu
65507-114	6539-023	Berg

*FCN-723J014/1 and 6539-023 are exchangeable.

Write Operation



Read Operation

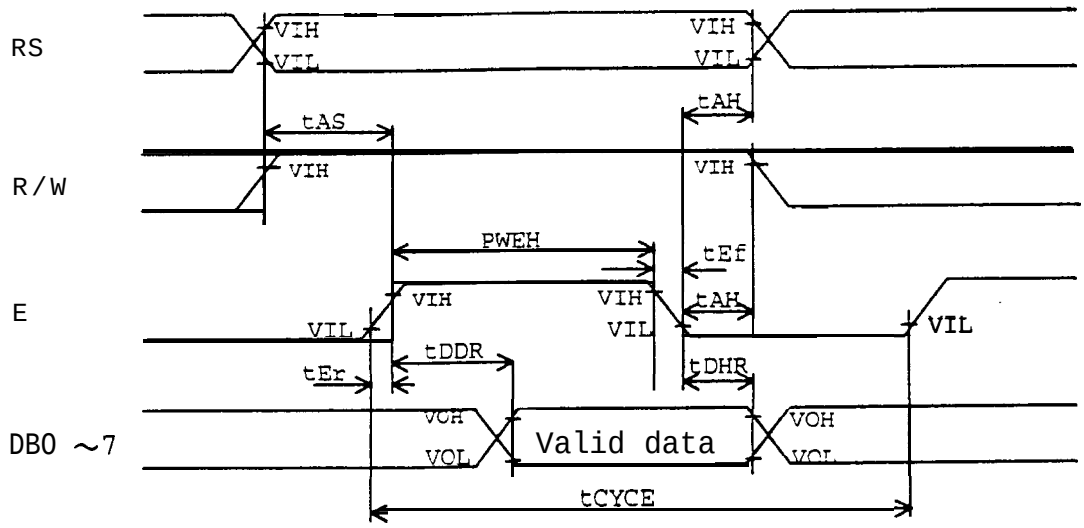


Fig.1 Timing Chart

5. Optical Characteristics

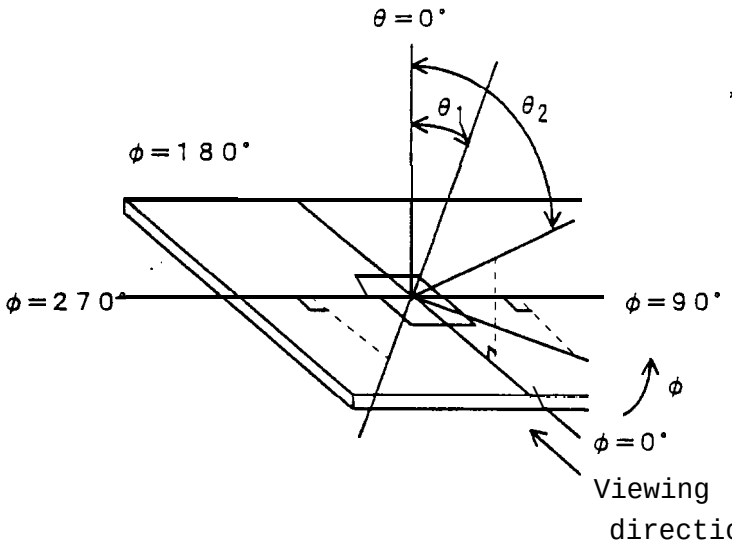
5.1 Table 6 shows the optical characteristics when LCD drive voltage is adjusted to the maximum contrast in $\theta = 15°$.

Table 6

(Ta=25℃)

Parameter		symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing angle range		$\theta_2-\theta_1$	$\phi=0°$ *$\theta_1<\theta_2$	Co≧2.0	30	-	-	dar.	Note 1
		θ_1		CO=2 .0	-	-	15	dgr.	Note 1
		θ_2			40	-	-		
		$\theta_2-\theta_1$	$\phi=45°$ 315° $\theta_1<\theta_2$	Co≧2.0	30	-	-	dgr.	Note 1
		θ_1		CO=2 .0	-	-	20	dgr .	Note 1
		θ_2			45	-	-		
Contrast ratio		Co	$\theta=15°$		2	3	-		Note 2
Response time	Rise	tr	$\theta=15°$		1 -	150	300	ms	Note 3
	Decay	td	$\theta=15°$			200	400	ms	Note 3

Note 1) The viewing angle range is defined as shown below.



*Angles θ_1 ,θ_2 andϕ shall fall within the range over which the displayed character can be read.

Fig.2 Definition of viewing angle

Note 2) Contrast ratio is defined as follows:
When input signal is applied to the unit to select(turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Fig.3.

$$\text{Contrast ratio} = \frac{\text{Photo-detector output voltage with non-select waveform being applied}}{\text{Photo-detector output voltage with select waveform being applied}}$$

Note 3) When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Fig.3. The response characteristics of the photo-detector output are measured as shown in Fig.4.

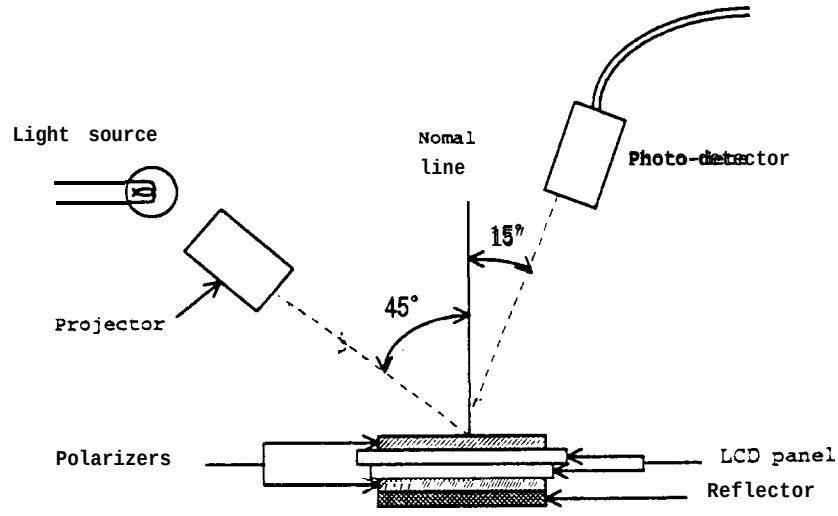
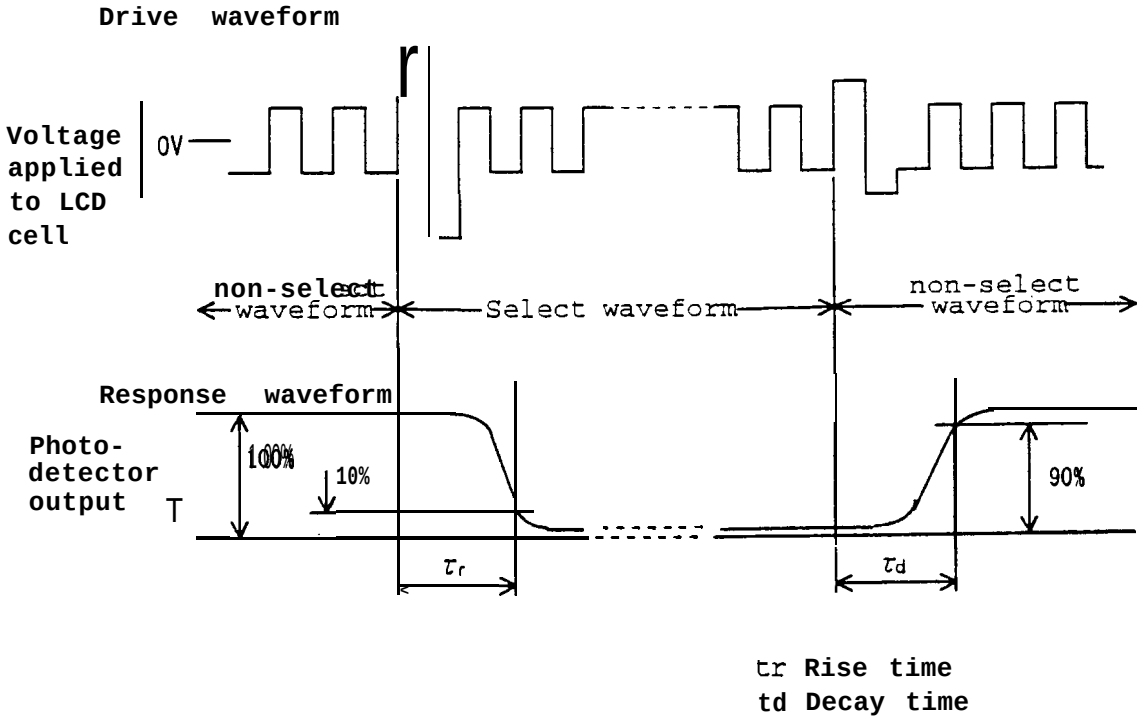


Fig.3 Optical Characteristics Test Method



tr Rise time
td Decay time

Fig.4 Definition of Response Time

6.Pin Description

1)VDD and VSS Pins

VDD and VSS pins are for power SUPPLY. VSS pin is grounded, and VDD pin is supplied with +5v. Each voltage necessary to drive LCD is generated in the module.

2)RS Pin

The controller LSI contains two 8-bit registers; instructions register (IR) and data register (DR) -
RS pin selects these registers. IR serves to store instruction codes for display clear, shift, etc. and address information for display data. RAM (DD W), character generator RAM (CG RAM); DR serves to temporarily store data to be written into DD RAM and CG RAM.

"0": Instruction register (write)
Busy flag register; address counter (read)
"l": Data register (read/writs)

3)R/W Pin

Read or write selection signal pin.

"0": Write
"l": Read

4)E Pin

Data read or write operation enable signal pin.

5)DB0~7 Pins

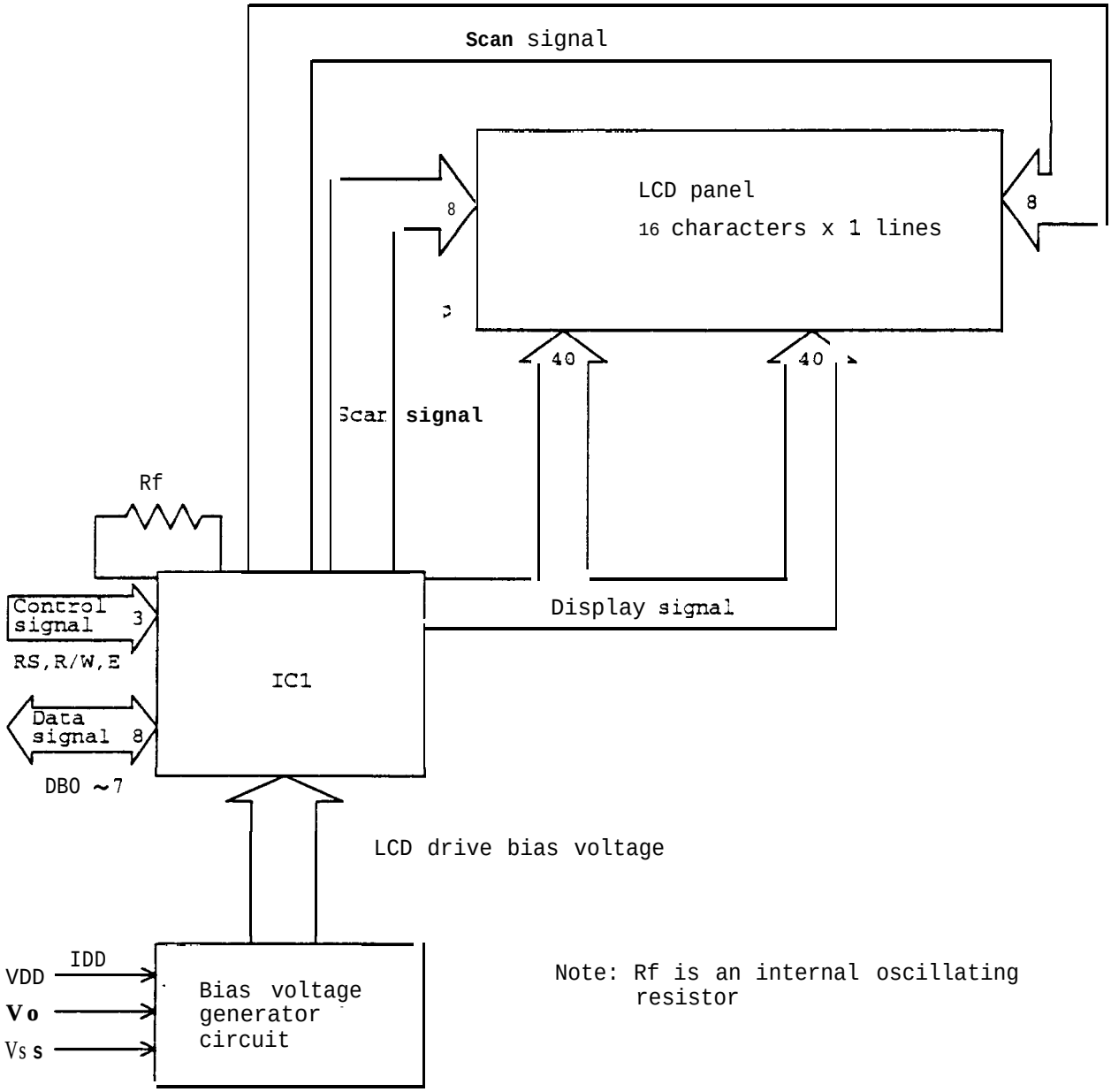
Tri-state bidirectional data bus pins- The bus allows data to be transmitted to or received from the external circuit. DB7 serves also as busy flag output. When the unit is interfaced to a microcomputer with 4-bit parallel outputs, DB0~3 Pins are not used.

6)V0 Pin

Viewing angle is varied and contrast is adjusted by changing input voltage between +5V~0V by applying bias voltage to the LCD driver.

Instruction	Code										Function
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Display clear	0	0	0	0	0	0	0	0	0	1	**Clear** entire display area, restore display from shift, and load address counter with DD RAM address 00H.
Display/ Cursor home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00H.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify display ON/OFF (D), cursor(C), and blinking of character at cursor position(B)
Display/ Cursor shift	0	0	0	0	0	1	S/C	R/L	*	*	shift display or move cursor.
Function set	0	0	0	0	1	DL	1	0	*	*	Set Interface data length.
CG RAM address set	0	0	0	1	ACG						Load the address counter with a CG RAM adderss. Subsequent data is CG RAM data.
DRAM address set	0	0	1	ADD							Load the address counter with a CG RAM adderss. Subsequent data is DD RAM data.
Busy flag/address counter read	0	1	BF	AC							Read busy flag(BF) and contents of address counter
CG RAM/DD RAM data write	1	0	Write data								Write data to CG RAM or DD RAM.
CG RAM/DD RAM data read	1	1	Read data								Read data from CG RAM or DD RAM.

I/D=1:Increment I/D=0:Decrement S/C=1:Shift display S/C=0:Move cursor
S =1:Shift display S =0:Freeze display R/L=1:Shift right R/L=0:Shift left
D =1:Display ON D =0:Display OFF DL=1:8-bit DL =0:4-bit
C =1:Cursor ON C =0:Cursor OFF BF=1:During internal operation BF =0:End of internal operation
B =1:Character at cursor position blinks B =0:Character at cursor position unblinks.

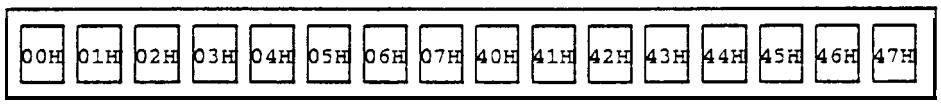


Note: Rf is an internal oscillating resistor

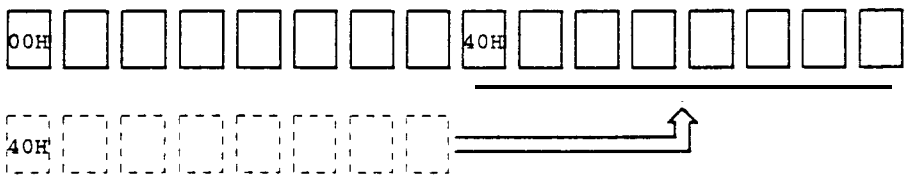
Fig.5 Block Diagram

Ic1 : ks0066F00 (SAMSUNG)

The display address is as follows when the display is not shifted.
The 2nd line's 8 characters in logic correspond to the 1st line's right half 8 characters in display because this module is driven by 1/16 duty.



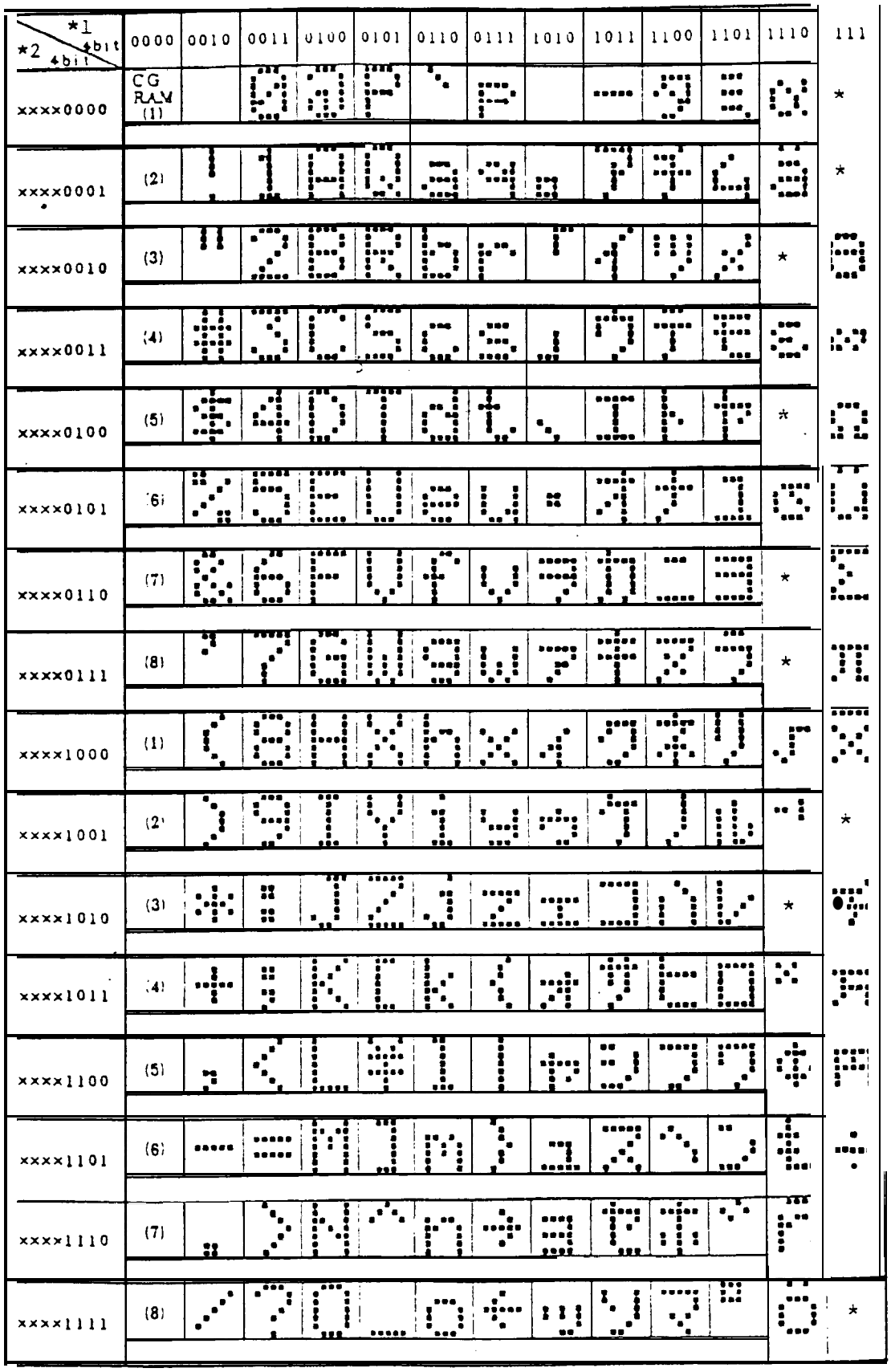
PHYSICAL ADDRESS



LOGICAL ADDRESS

Fig.6 Display Address

Table 8. Input Code vs. Character Pattern



*1 High-order *2 Low-order *: Prohibition of Input

Note) CG RAM is character generator RAM in which user-definable character patterns are stored.

SHARP

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設計通知 DRAWING INFO 連絡書 INFORMATION

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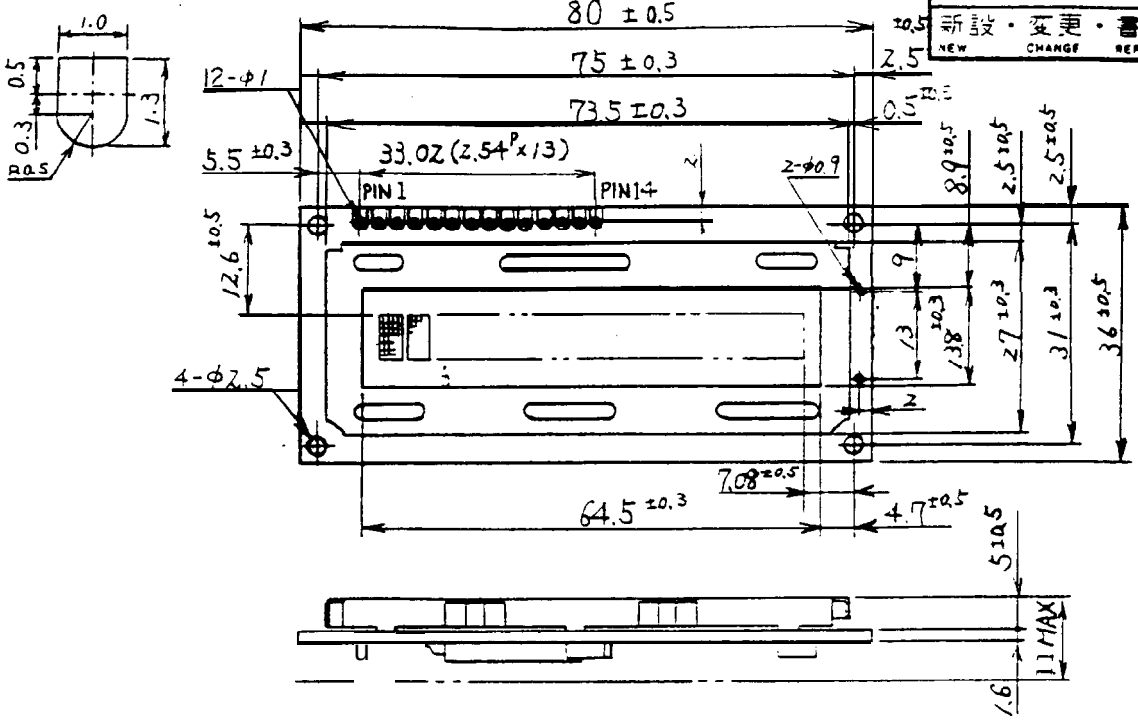
新設・変更・書換 NEW CHANGE REPLACE 図面

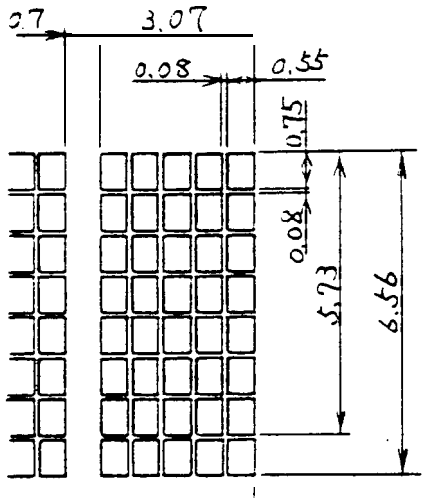
PIN1 and PIN3 Details

(S=10/1)



*	**
1	V_{SS}
2	V_{DD}
3	V_O
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7

* Pin No.
** Display signal



Character pattern Details

62

Fig. 7 Unit Outline Dimensions and Pin Connections

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19 . .					LM161556	名称 NAME	Outline Dimensions and Pin Connections
19 . .					LM16155		
年月日 DATE	訂正記事 REVISE		設通No.	担当 PREPA	適用機種 MODEL		
材質 MATERIAL	板厚 THICKNESS	仕上 FINISH			尺度 SCALE 1/1	記号 SYMBOL	
						部品コード PARTS CODE	

設計 DSGN	製図 DRWN	検図 CHECK	検図 CHECK	承認 APPROVE	シャープ株式会社	作成日付 DATE	1985 . 1 . 8 .
					SHARP CORPORATION	図番 DRAWING No.	OD16155-001
					作成部門 LCD Division		

様式番号 11-A 1